400G 光模块测试

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Keysight Technology

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KEYSIGHT TECHNOLOGIES

400G 光模块种类

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光口	光口速率	传输方式	规范	电口速率	封装
400G-SR16	16*26.5Gbps NRZ	100m MM	802.3bs	16*26.5Gbps NRZ	CDFP/CFP8
400G-FR8	8λ*53Gbps PAM4	2km SM	802.3bs	8*53Gbps PAM4	QSFP DD / OSFP
400G-LR8	8λ*53Gbps PAM4	10km SM	802.3bs	8*53Gbps PAM4	QSFP DD / OSFP
400G-SR8	8*53Gbps PAM4	100m? MM	802.cm?	8*53Gbps PAM4	QSFP DD / OSFP
400G-SR4.2	4*2λ*53Gbps PAM4	100m? MM(2λ)	802.3cm?	8*53Gbps PAM4	QSFP DD / OSFP
400G-DR4	4*106Gbps PAM4	500m SM	802.3bs	8*53Gbps PAM4	QSFP DD / OSFP
400G-FR4	4λ*106Gbps PAM4	2km SM	100G/λ MSA	8*53Gbps PAM4	QSFP DD / OSFP
400G-LR4	4λ*106Gbps PAM4	10km SM	TBD	8*53Gbps PAM4	QSFP DD / OSFP
400G-ZR	DWDM + 59.8Gbd DP-16QAM	>80km DWDM	OIF	----	QSFP DD ??

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200G/100G/50G 光模块种类（PAM4）

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光口	光口速率	传输方式	规范	电口速率	封装
200G-SR4	4*53Gbps PAM4	100m MM	802.3cd	4*53Gbps PAM4 8*26.5Gbps NRZ	QSFP56 /QSFP DD
200G-DR4	4*53Gbps PAM4	500m SM	802.3bs	4*53Gbps PAM4 8*26.5Gbps NRZ	QSFP56 /QSFP DD
200G-FR4	4λ*53Gbps PAM4	2km SM	802.3bs	4*53Gbps PAM4 8*26.5Gbps NRZ	QSFP56 /QSFP DD
200G-LR4	4λ*53Gbps PAM4	10km SM	802.3bs	4*53Gbps PAM4 8*26.5Gbps NRZ	QSFP56 /QSFP DD
100G-SR2	2*53Gbps PAM4	100m? MM	802.3cd	2*53Gbps PAM4 4*26.5Gbps NRZ	SFP DD /QSFP28
100G-DR	1*106Gbps PAM4	500m SM	802.3cd	2*53Gbps PAM4 4*26.5Gbps NRZ	SFP DD /QSFP28
50G-SR	1*53Gbps PAM4	100m MM	802.3cd	1*53Gbps PAM4	SFP56
50G-FR	1*53Gbps PAM4	2km SM	802.3cd	1*53Gbps PAM4	SFP56
50G-LR	1*53Gbps PAM4	10km SM	802.3cd	1*53Gbps PAM4	SFP56

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400G - SR8

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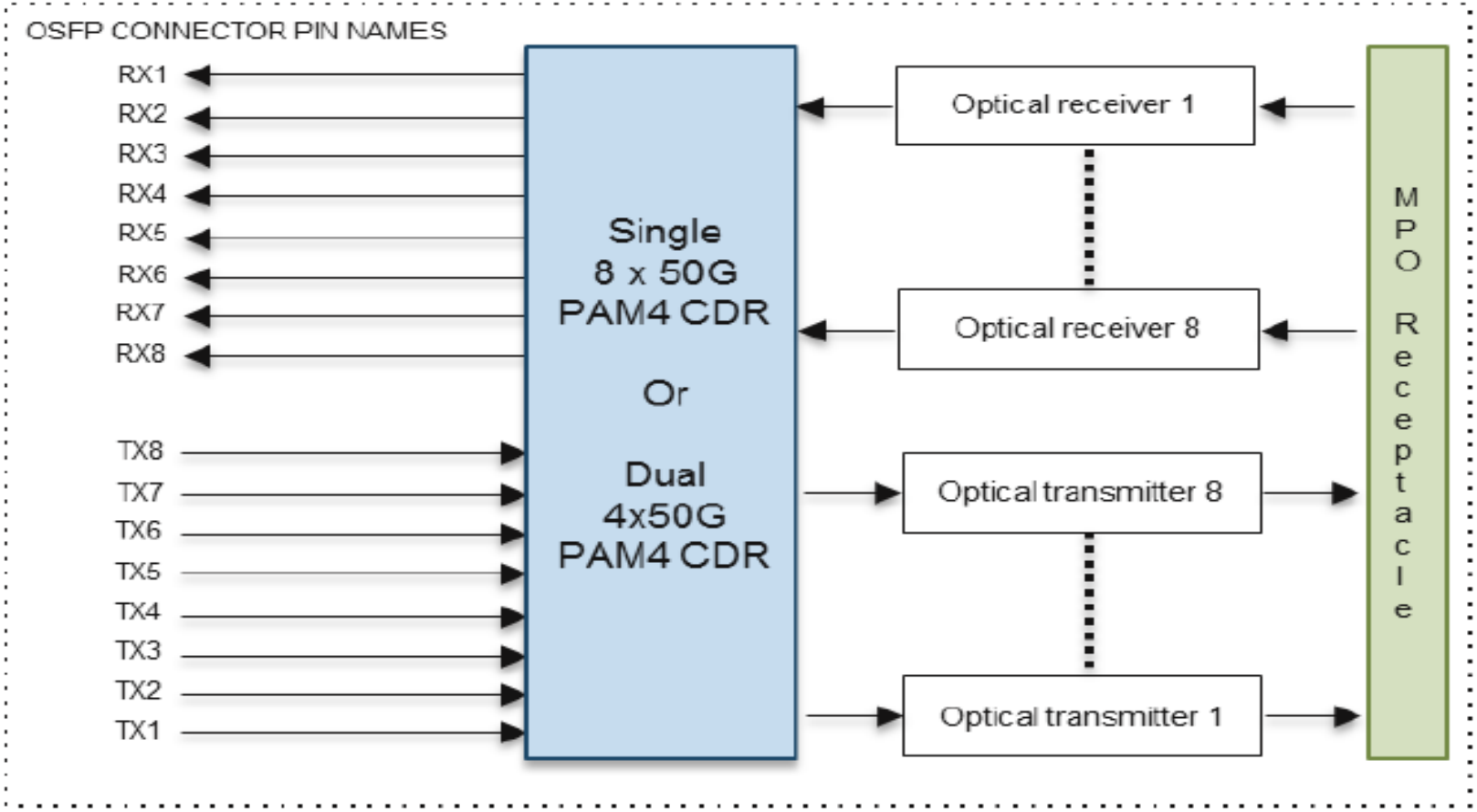
Optical PMD for Parallel Fiber: 400G SR8



Source： **OSFP MSA** Specification for OSFP OCTAL SMALL FORM FACTOR PLUGGABLE MODULE

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400G - FR8/LR8

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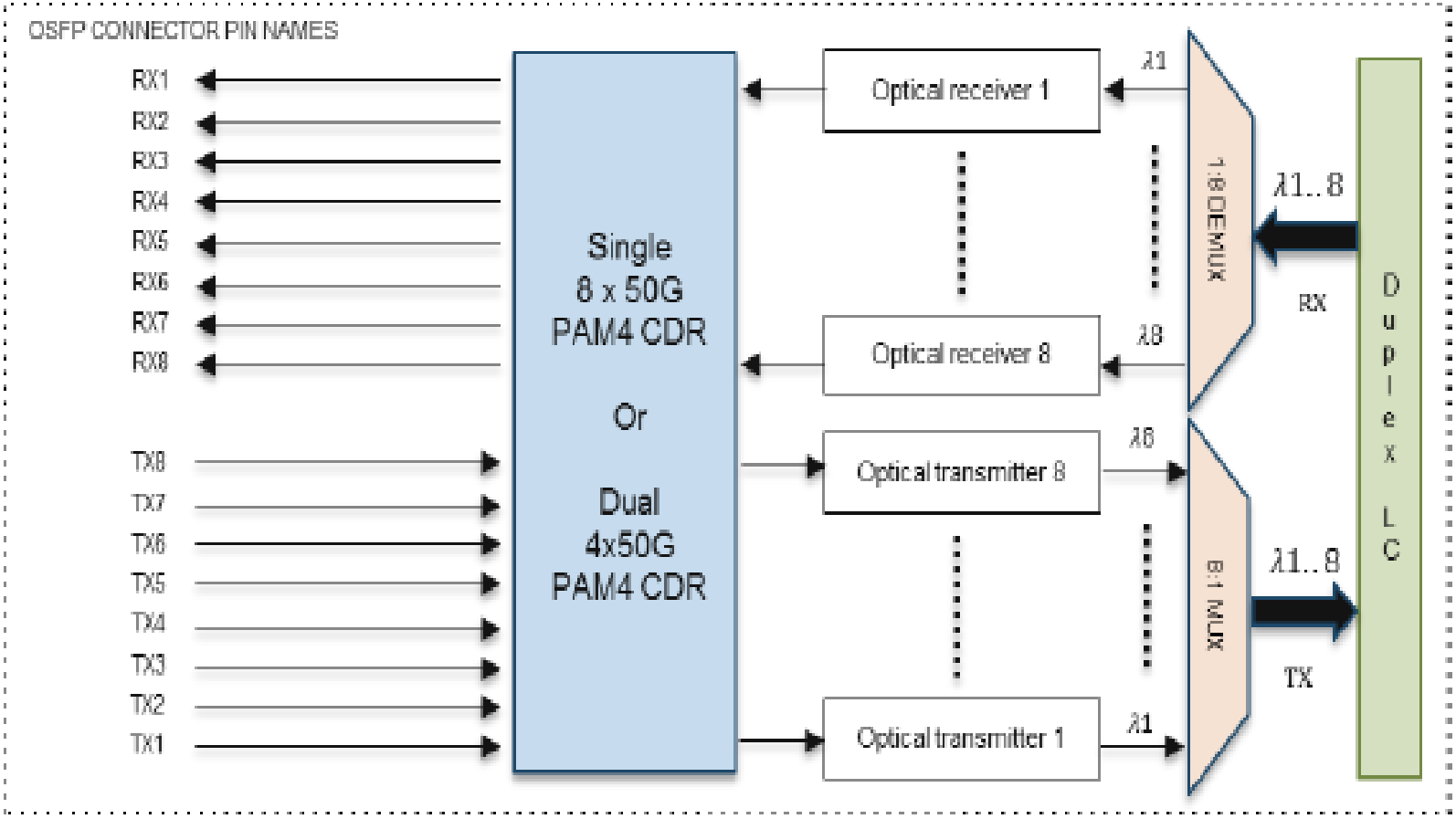
Optical PMD for 400G-FR8/LR8



Source： **OSFP MSA** Specification for OSFP OCTAL SMALL FORM FACTOR PLUGGABLE MODULE

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400G – FR4

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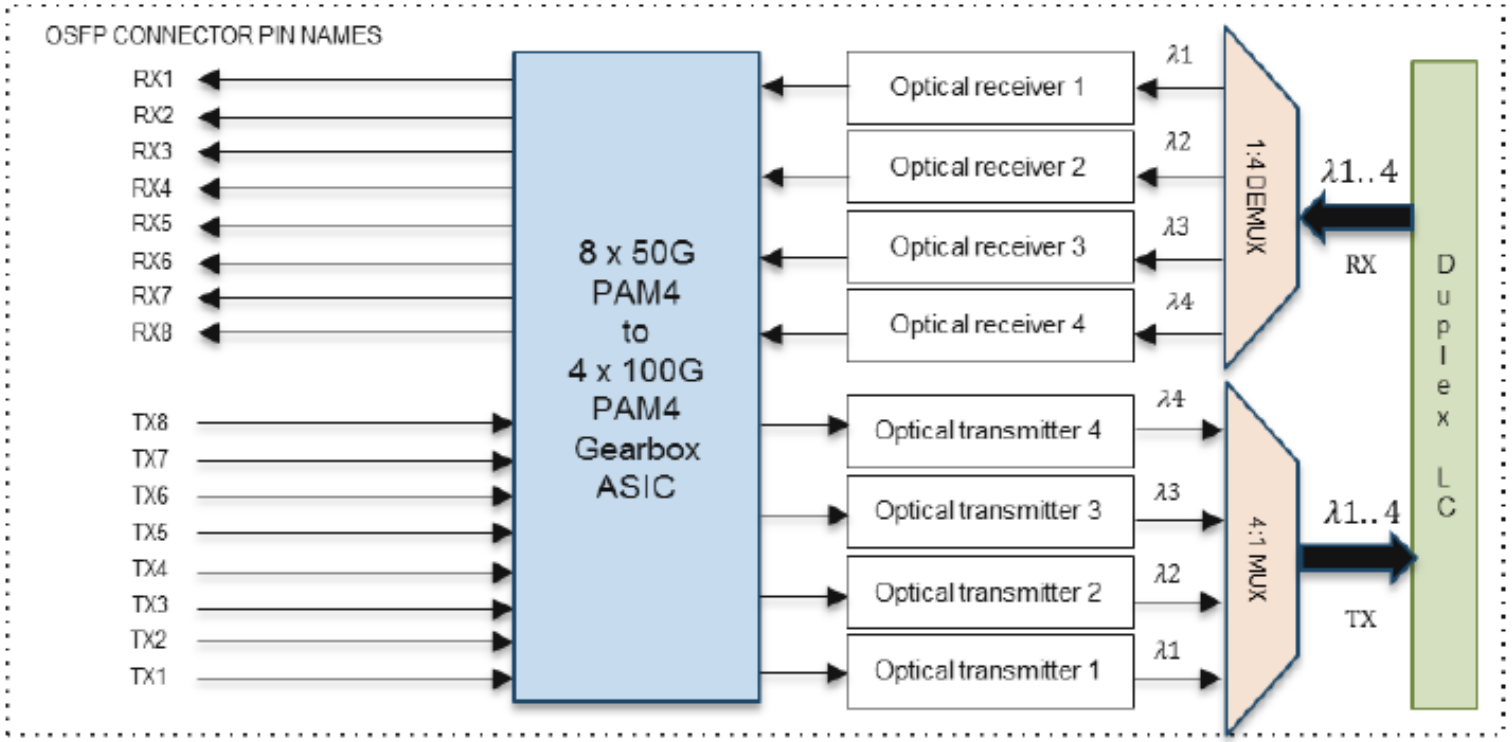
Optical PMD for 400G-FR4, Duplex Fiber



Source： **OSFP MSA** Specification for OSFP OCTAL SMALL FORM FACTOR PLUGGABLE MODULE

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400G光模块相关规范

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400G光模块主要参考规范如下：

- 400G-SR16/FR8/LR8/DR4：IEEE 802.3bs-2017; IEEE 802.3cd;
- 400G-SR8/SR4.2：IEEE 802.3cm (TBD)
- 400G-FR4: 400G-FR4 Technical Specification

封装规范：

- CDFP MSA Releases Rev. 3.0 Specifications for 400 Gbps Interoperable Hot Pluggable Modules
- CFP8 Hardware Specification
- OSFP OCTAL SMALL FORM FACTOR PLUGGABLE MODULE
- QSFP-DD Hardware Specification for QSFP DOUBLE DENSITY 8X PLUGGABLE TRANSCEIVER
- SFF-8636 Specification for Management Interface

400G光模块测试项目列表

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400G光模块测试项目列表					
光发射机	光功率（dbm）	OMAouter（dbm）	TDECQ（db）max	ER（db）min	RIN（db/Hz）max
光接收机	接收灵敏度（dbm）	光压力眼			
电发射机	上升时间（ps）min	近端ESMW（UI）min	近端眼高（mV）min	远端ESMW（UI）min	远端眼高（mV）min
电接收机	正弦抖动容限	电压力眼			
系统测试	PreFEC误码率	丢包率	PostFEC错误注入	线速率PPM容限	管理信息

Spec　FYI　Future

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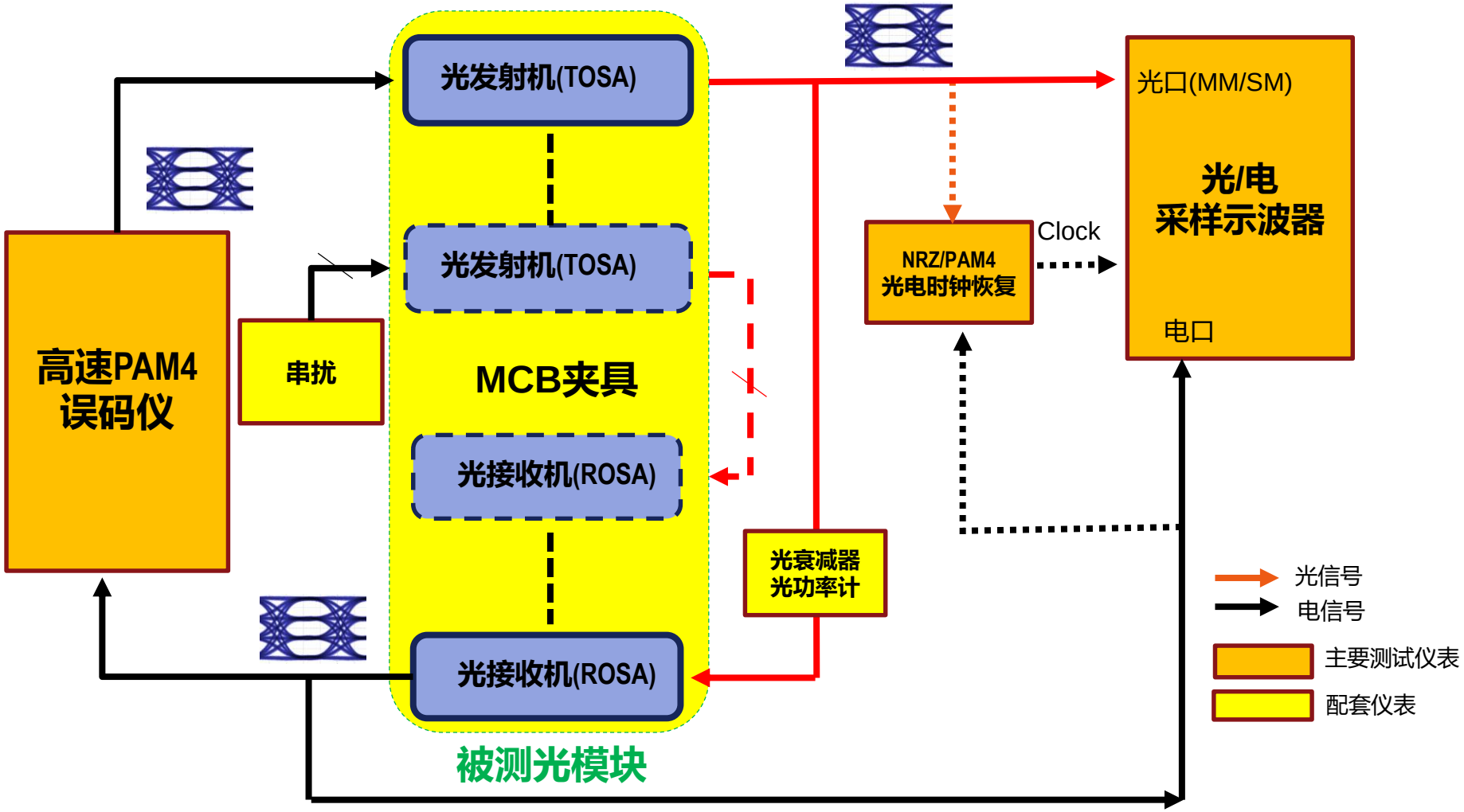


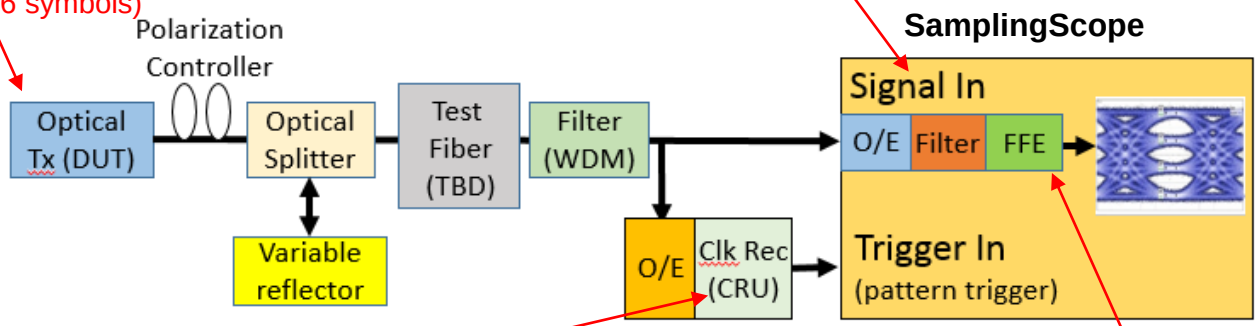
光眼图及TDECQ 测试 (Transmitter and dispersion eye closure)

- TDECQ is a measure of each optical transmitter's vertical eye closure when transmitted through a worst case optical channel (TDECQ units = dB) using SSPRQ pattern.

Reference Receiver: 4th order Bessel-Thomson low-pass filter (Oscilloscope noise measured and mathematically 'backed out' per Standard).

- MM: 12.6 GHz BW (26.56 GBd)
  - No Pol. controller, fiber
- SM: 19.34 GHz BW (26.56 GBd)
- SM: 38.68 GHz BW (53 GBd)

Generate SSPRQ pattern (~ 2^16 symbols)

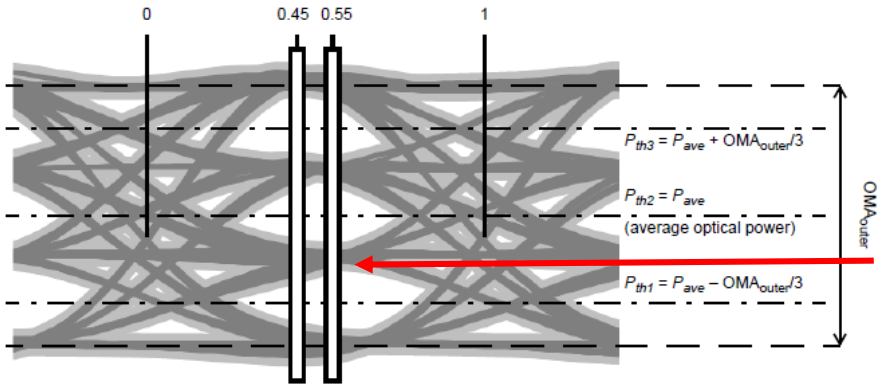


CR PLL BW 4 MHz, Slope 20 dB/dec (1st Order, no peaking)

Equalizer (5 tap, T/2 spaced, FFE)

$$TDECQ = 10\log_{10}\left(\frac{OMA_{outer}}{6} \times \frac{1}{Q_t R}\right)$$

Where:
Qt = 3.414 (target SER)
R = noise term



Targeted samples on PAM-4 eye diagram.

Reference: IEEE P802.3bs™

光口发射机测试结果

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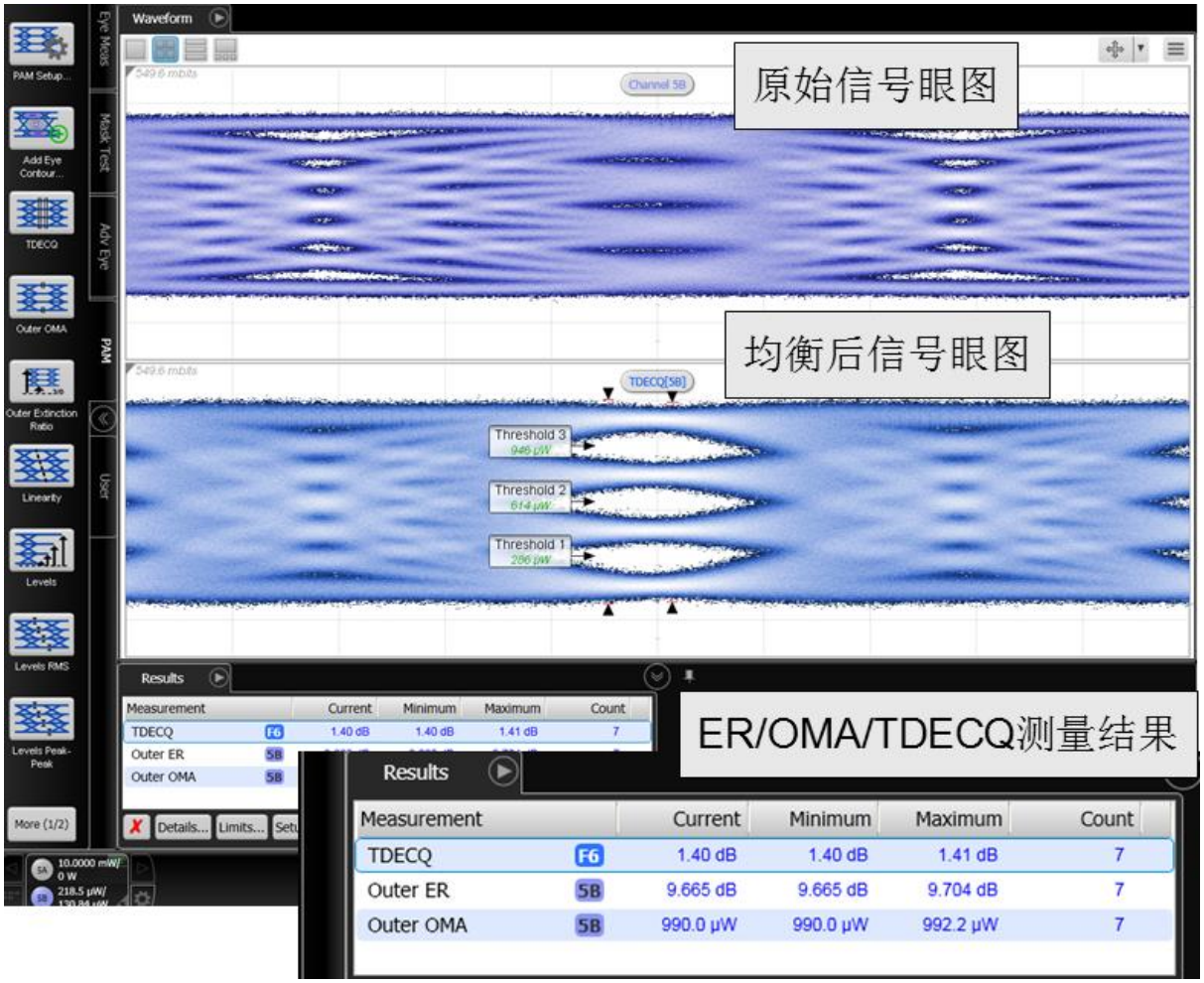
- Extinction ratio and OMA are derived from the 0 and 3 levels of the transmitter output
  - Specific bit sequences are used
- TDECQ derived from the equalized waveform
  - Uses OMA from the unequalized waveform (may change to equalized waveform)



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电口测试方法

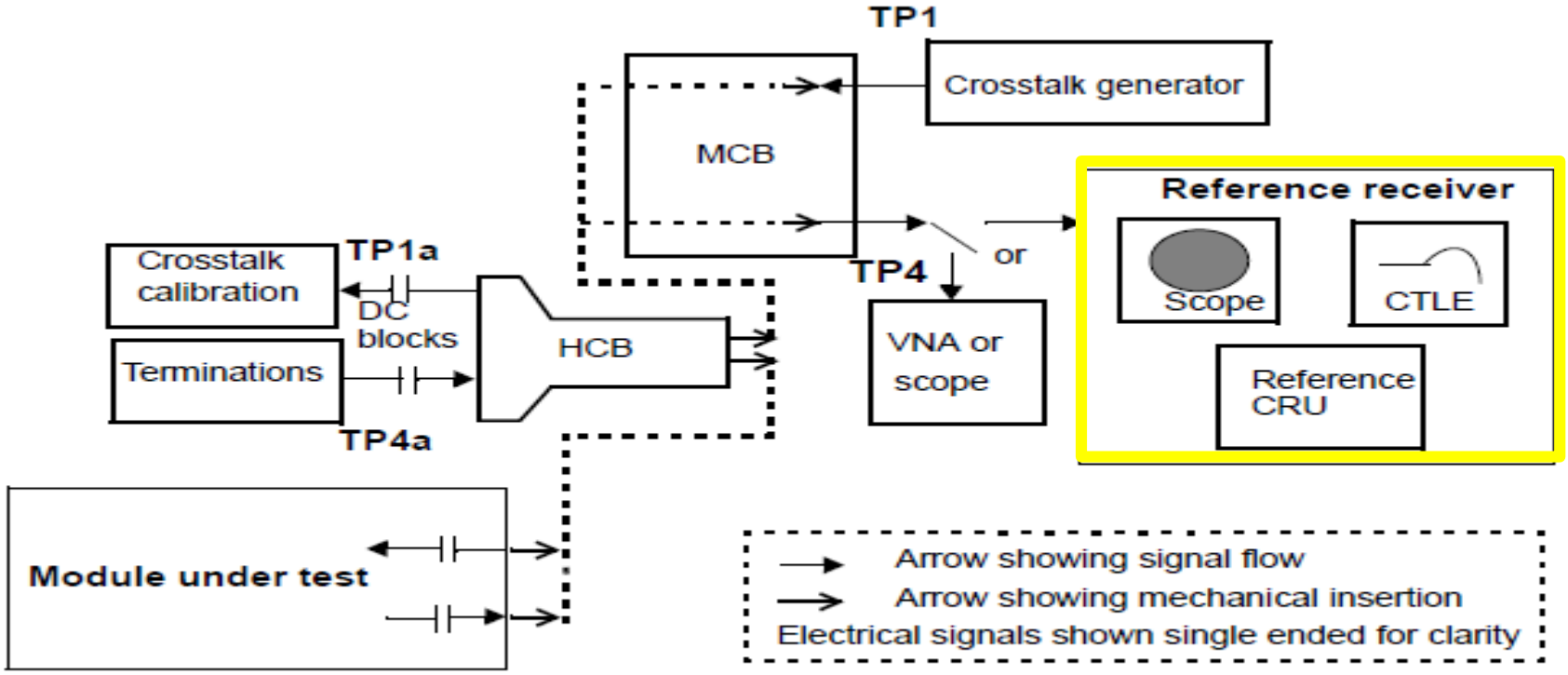

Figure 120E–10—Example module output test configuration

A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all output signal measurements, unless otherwise specified.

Source： **IEEE** 802.3bs

电眼图测试方法

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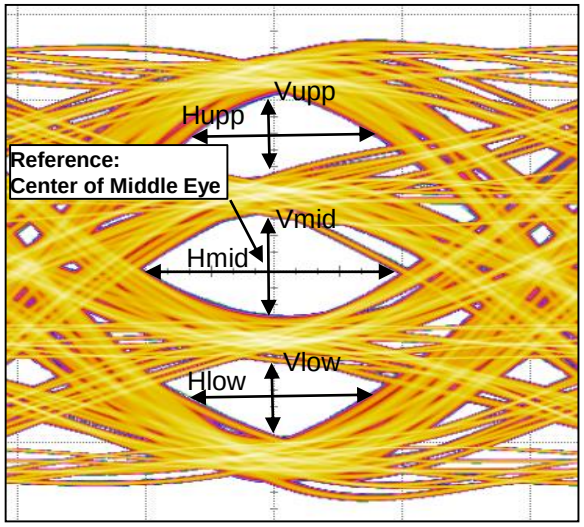
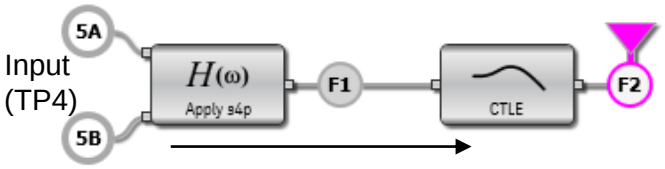
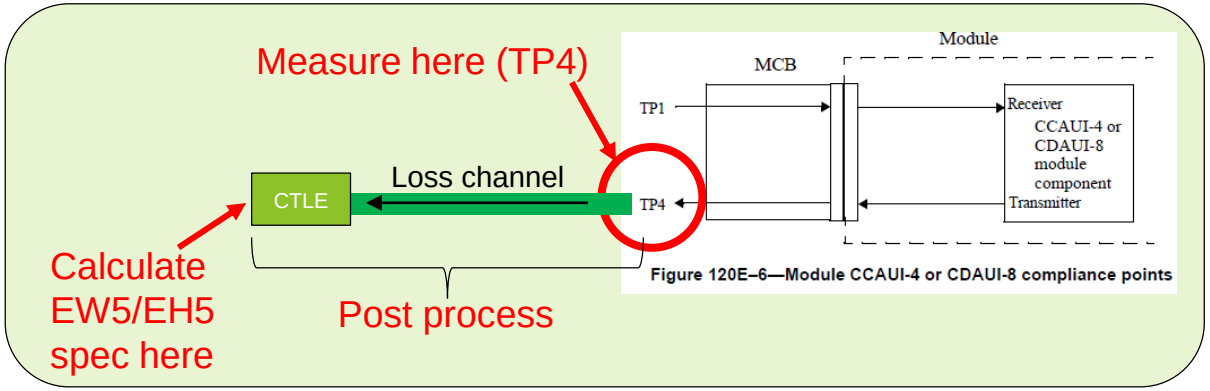
120E.3.2.1 Module output eye width and eye height

- Measure EW/EH of all 3 PAM-4 eyes @ 1E-5 using methodology outlined in 120E.4.2
  - Measure Near-end EW5/EH5 (with Max 3dB CTLE peaking)
  - Measure Far-end after convolving with loss channel (~ 6.4 dB loss at Nyquist defined in 92.10.7.1.1, use any CTLE per Table 120E-2 (max 9dB)
- **Measurement Setup:**
  - Reference Rcvr: 4th order BT, 33 GHz BW
  - CR: 4 MHz BW, 20dB/dec
  - Use CTLE (3 pole) defined in 120E.3.1.7
  - PRBS13Q pattern







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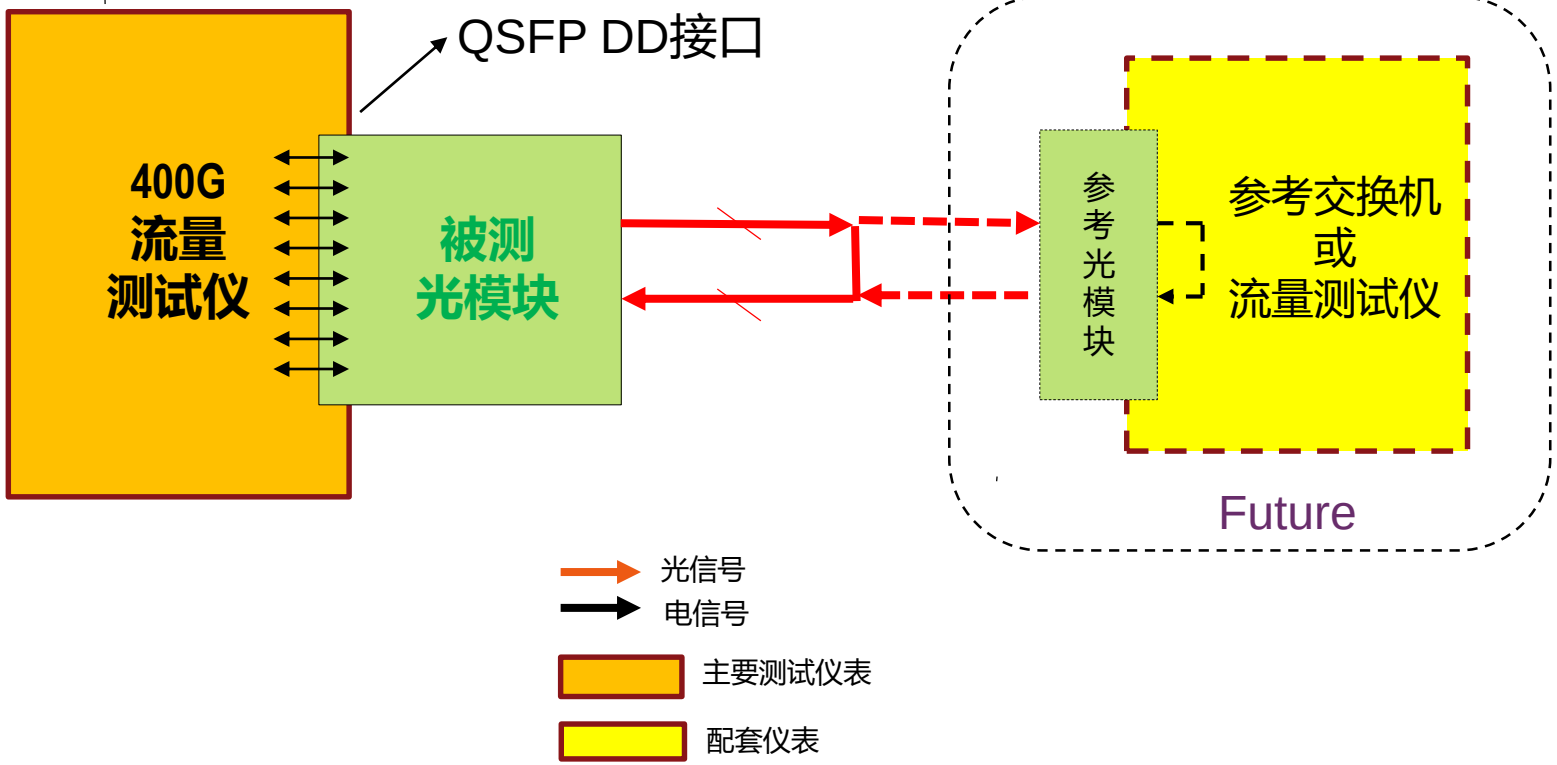

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Pre-FEC误码率、误包率测试

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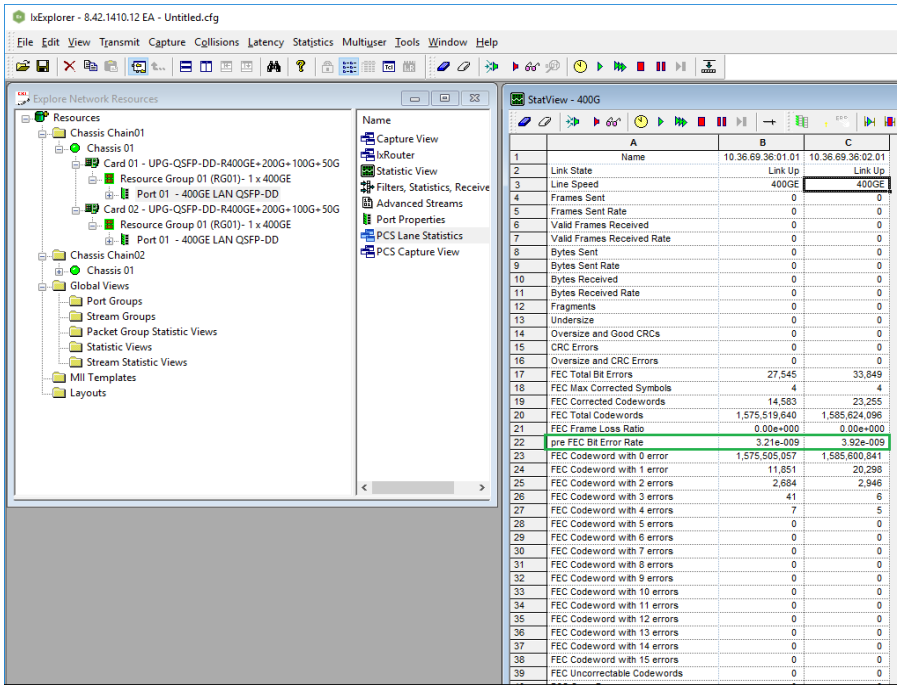
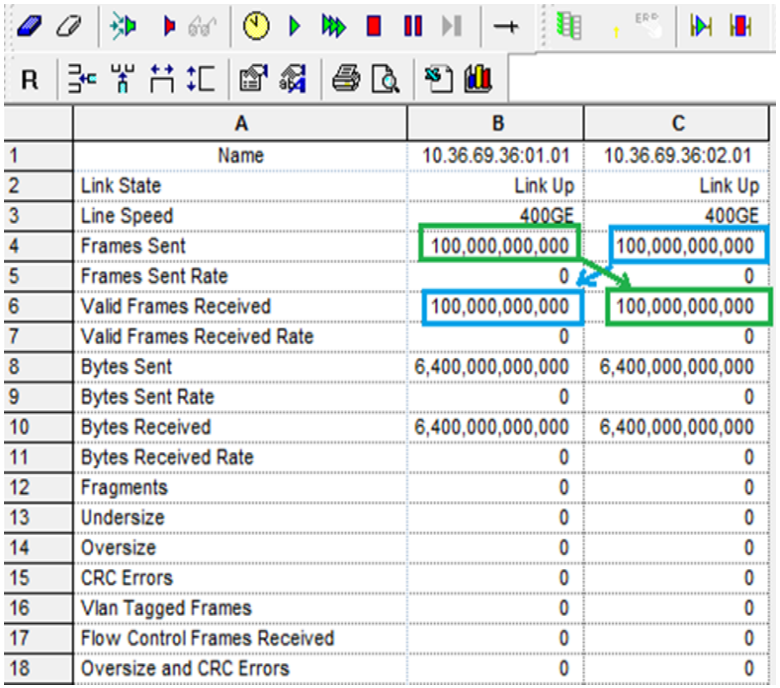
124.1.1 Bit error ratio

The bit error ratio (BER) when processed according to Clause 120 shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.223) of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap when processed according to Clause 120 and then Clause 119. For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-11} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.



	A	B	C
1	Name	10.36.69.36:01.01	10.36.69.36:02.01
2	Link State	Link Up	Link Up
3	Line Speed	400GE	400GE
4	Frames Sent	0	0
5	Frames Sent Rate	0	0
6	Valid Frames Received	0	0
7	Valid Frames Received Rate	0	0
8	Bytes Sent	0	0
9	Bytes Sent Rate	0	0
10	Bytes Received	0	0
11	Bytes Received Rate	0	0
12	Fragments	0	0
13	Undersize	0	0
14	Oversize and Good CRCs	0	0
15	CRC Errors	0	0
16	Oversize and CRC Errors	0	0
17	FEC Total Bit Errors	27,545	33,849
18	FEC Max Corrected Symbols	4	4
19	FEC Corrected Codewords	14,583	23,255
20	FEC Total Codewords	1,575,519,640	1,585,624,096
21	FEC Frame Loss Ratio	0.00e+000	0.00e+000
22	pre FEC Bit Error Rate	3.21e-009	3.92e-009
23	FEC Codeword with 0 error	1,575,505,057	1,585,600,841
24	FEC Codeword with 1 error	11,851	20,298
25	FEC Codeword with 2 errors	2,684	2,946
26	FEC Codeword with 3 errors	41	6
27	FEC Codeword with 4 errors	7	5
28	FEC Codeword with 5 errors	0	0
29	FEC Codeword with 6 errors	0	0
30	FEC Codeword with 7 errors	0	0
31	FEC Codeword with 8 errors	0	0
32	FEC Codeword with 9 errors	0	0
33	FEC Codeword with 10 errors	0	0
34	FEC Codeword with 11 errors	0	0
35	FEC Codeword with 12 errors	0	0
36	FEC Codeword with 13 errors	0	0
37	FEC Codeword with 14 errors	0	0
38	FEC Codeword with 15 errors	0	0
39	FEC Uncorrectable Codewords	0	0



	A	B	C
1	Name	10.36.69.36:01.01	10.36.69.36:02.01
2	Link State	Link Up	Link Up
3	Line Speed	400GE	400GE
4	Frames Sent	100,000,000,000	100,000,000,000
5	Frames Sent Rate	0	0
6	Valid Frames Received	100,000,000,000	100,000,000,000
7	Valid Frames Received Rate	0	0
8	Bytes Sent	6,400,000,000,000	6,400,000,000,000
9	Bytes Sent Rate	0	0
10	Bytes Received	6,400,000,000,000	6,400,000,000,000
11	Bytes Received Rate	0	0
12	Fragments	0	0
13	Undersize	0	0
14	Oversize	0	0
15	CRC Errors	0	0
16	Vlan Tagged Frames	0	0
17	Flow Control Frames Received	0	0
18	Oversize and CRC Errors	0	0

KEYSIGHT TECHNOLOGIES

Source： **IEEE** 802.3bs

Post-FEC错误注入、线速率PPM容限

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45.2.3.47h PCS FEC symbol error counter lane 0 (Register 3.600, 3.601)

The assignment of bits in the PCS FEC symbol error counter lane 0 register is shown in Table 45–160h. Symbol errors detected in PCS lane 0 are counted and shown in register 3.600.15:0 and 3.601.15:0. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 3.600, 3.601 are used to read the value of a 32-bit counter. When registers 3.600 and 3.601 are used to read the 32-bit counter value, the register 3.600 is read first, the value of the register 3.601 is latched when (and only when) register 3.600 is read, and reads of register 3.601 return the latched value rather than the current value of the counter.

Table 45–160h—PCS FEC symbol error counter lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.600.15:0	PCS FEC symbol errors, lane 0 lower	FEC_symbol_error_counter_0[15:0]	RO, NR
3.601.15:0	PCS FEC symbol errors, lane 0 upper	FEC_symbol_error_counter_0[31:16]	RO, NR

[a] RO = Read only, NR = Non Roll-over

45.2.3.47i PCS FEC symbol error counter lane 1 through 15 (Registers 3.602 through 3.631)

The behavior of the PCS FEC symbol error counters, lane 1 through 15 is identical to that described for PCS lane 0 in 45.2.3.47h. Errors detected in each PCS lane are counted and shown in the corresponding register. PCS lane 1, lower 16 bits are shown in register 3.602; PCS lane 1, upper 16 bits are shown in register 3.603; PCS lane 2, lower 16 bits are shown in register 3.604; through register 3.631 for PCS lane 15, upper 16 bits.

120E.3.1.1 Signaling rate and range

The 200GAUI-4 and 400GAUI-8 C2M signaling rate is 26.5625 GBd ± 100 ppm per lane. This translates to a nominal unit interval of 37.647059 ps.

Source： **IEEE** 802.3bs

管理信息（FYI）

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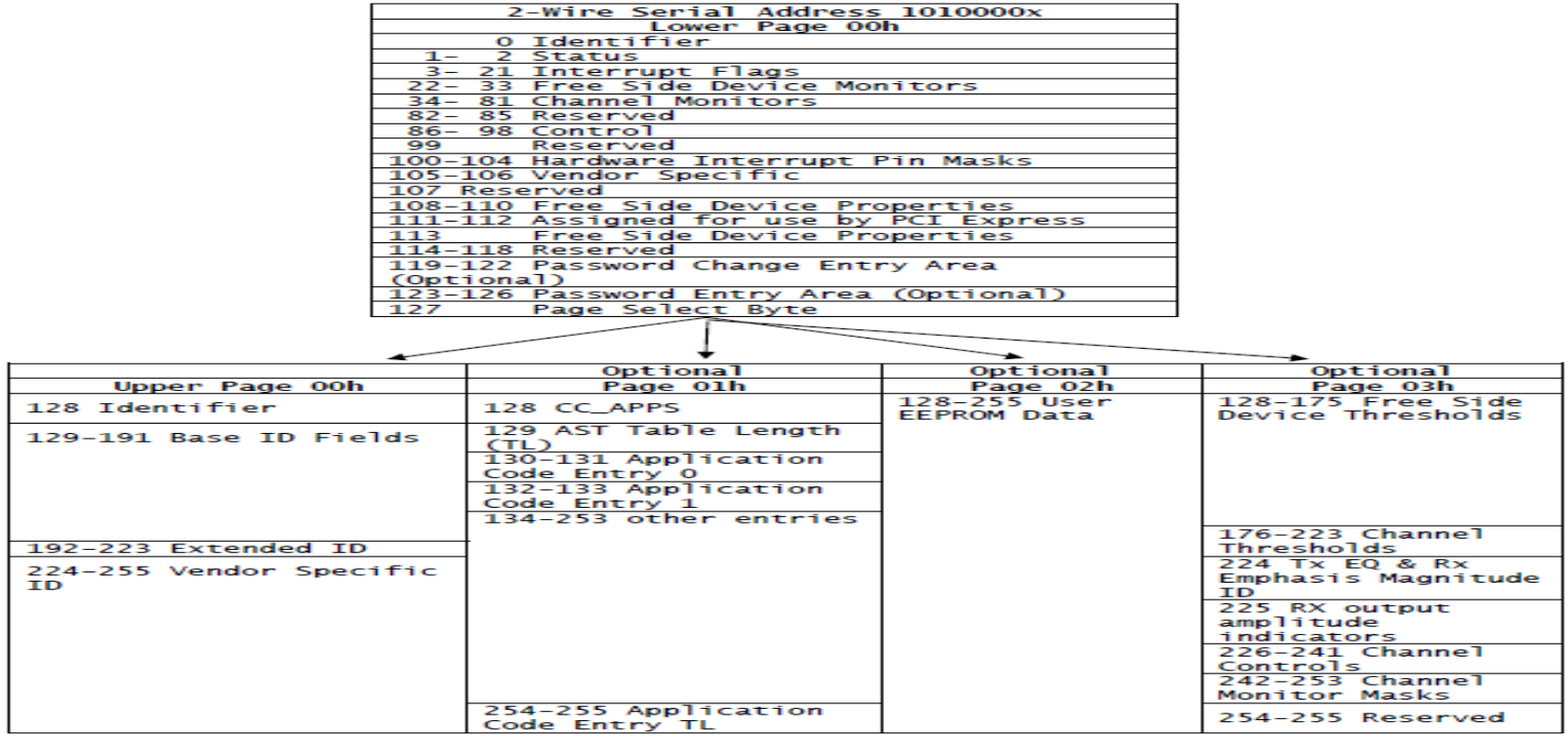

FIGURE 6-1 COMMON MEMORY MAP

7 Management Interface

A management interface, as already commonly used in other form factors like QSFP, SFP, and CDFP, is specified in order to enable flexible use of the module by the user. This QSFP-DD specification is based on SFF-8636 but with modifications to support an 8-channel module, and as such is not directly backwards compatible with SFF-8636. Some timing requirements are critical, especially for a multi-channel device, so the interface speed may optionally be increased. Byte 00 on the Lower Page or Address 128 Page 00 is used to indicate the use of the QSFP-DD memory map rather than the QSFP memory map. When a legacy QSFP28 module is inserted into a QSFP-DD port the legacy QSFP memory map (i.e. SFF-8636) must be used. This case is outside the scope of this document.

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Source： **SFF Committee** SFF-8636 Specification for Management Interface for Cabled Environments

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测试设备列表

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设备名称	功能	要求
误码仪	产生1～2路激励电信号；误码率测试；抖动容限测试。	双通道、PAM4/NRZ信号产生和误码率检测，支持RJ/SJ注入、预加重、线性度调整。
采样示波器	测试光模块输出光眼图和电参数质量；接收测试中信号校准。	支持光口、电口输入，NRZ/PAM4眼图参数抖动测试。支持光/电时钟恢复。
串扰信号发生器	用于产生多路串扰信号进行眼图和误码率测试。	至少2通道NRZ/PAM4信号产生，幅度/上升时间可调。
400G流量测试仪	插入被测光模块，进行误码、丢包率、链路测试。	支持400G误码和丢包率测试，FEC误码注入，链路建立状态和管理信息读取。
光功率计、可调衰减器	发射/接收光功率光功率测试	用于功率和接收灵敏度测试
MCB夹具	把被测光模块接口转接成标准同轴接口，光模块供电和控制。	由被测光模块厂商提供；可保证被测光模块正常工作。
合波器/分波器，光纤跳线	对采用CWDM技术的光模块各波长信号提取、分配；MPO光纤分配转接。	由被测光模块厂商提供；可把被测波长信号转为FC/PC接口。

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400G 光模块测试申请表

送测人信息	姓名：	邮箱：	电话：
	公司：	地址：	
被测光模块信息	产品型号		
	电气标准	□400G-SR8 □400G-FR8 □400G-LR8 □400G-DR4 □400G-FR4 □400G-LR4 □200G-SR4 □200G-DR4 □200G-FR4 □200G-LR4 □其它(需进一步确认) :	
	物理规格	□QSFP-DD □OSFP □其它(需进一步确认): 说明：目前系统测试项目仅针对QSFP-DD被测件。	
	MCB夹具	□可以提供 □不能提供(放弃部分电气测试项目) □其它方法产生信号(需进一步确认): 说明：电气测试项目需要用MCB夹具进行电信号激励和引出。	
	CWDM分波器、光纤跳线	□可以提供 □不能提供(放弃部分电气测试项目) 说明：电气测试项目需要把被测波长光信号转成FC/PC接口连接仪器。	